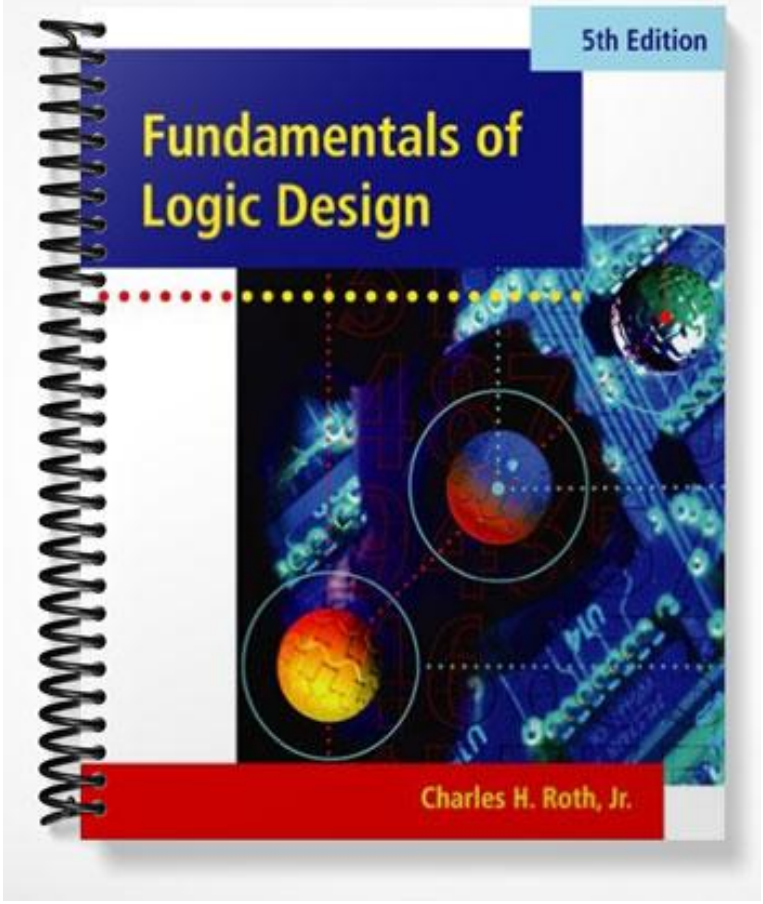
SOLUTIONS MANUAL



Instructor's Manual for
Fundamentals of Logic Design, 5th Ed.

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Brooks/Cole Publishing

Printed in the United States of America
5 4 3 2 1
ISBN ----------

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I: INTRODUCTION

The text, *Fundamentals of Logic Design, 5th edition,* has been designed so that it can be used either for a standard lecture course or for a self-paced course. The text is divided into 20 study units in such a way that the average study time for each unit is about the same. The units have undergone extensive class testing in a self-paced environment and have been revised based on student feedback. Study guides and text material were expanded as required so that almost all students can achieve mastery of all of the objectives. For example, the material on Boolean algebra and algebraic simplification was expanded from 1½ units to 2½ units because students found this topic difficult. A separate unit was added on going from problem statements to state graphs because this topic was difficult for many students.

The textbook contains answers for all of the problems that are assigned in the study guides. This *Instructor's Manual* contains complete solutions to these problems. Solutions to the remaining homework problems as well as all design and simulation exercises are also included in this manual. In the solutions section of this manual, the abbreviation FLD stands for *Fundamentals of Logic Design* (5th ed.).

Information on the self-paced course we teach using the textbook is available at www.ece.utexas.edu/projects/ee316. This website also links to an updated errata list for the text. In addition to the textbook and study guides, teaching a self-paced course requires that a set of tests be prepared for each study unit. This manual contains a sample test for each unit.

1.1 Using the Text in a Lecture Course

Even though the text was developed in a self-paced environment, the text is well suited for use in a standard lecture course. Since the format of the text differs somewhat from a conventional text, a few suggestions for using the text in a lecture course may be appropriate. Except for the inclusion of objectives and study guides, the units in the text differ very little from chapters in a standard textbook. The study guides contain very basic questions, while the problems at the end of each unit are of a more comprehensive nature. For this reason, we suggest that specific study guide questions be assigned for students to work through on their own before working out homework problems selected from those at the end of the unit. The unit tests given in Part 4 of this manual provide a convenient source of additional homework assignments or a source of quiz problems. The text contains many examples that are completely worked out with detailed step-by-step explanations. Discussion of these detailed examples in lecture may not be necessary if the students study them on their own. The lecture time is probably better spent discussing general principles and applications as well as providing help with some of the more difficult topics. Since all of the units have study guides, it would be possible to assign some of the easier topics for self-study and devote the lectures to the more difficult topics.

Working with a class composed largely of Electrical Engineering and Computer Science sophomores and juniors, we cover the 18 units (all units except 6 and 19) of the text in one semester. Units 8, 10, 12, 16, 17, and 20 contain design problems that are suitable for simulation and lab exercises. The design problems help tie together and review the material from a number of preceding units. Units 10, 17, and 20 introduce the VHDL hardware description language. These units may be omitted if desired since no other units depend on them.

1.2 Some Remarks About the Text

In this text, students are taught how to use Boolean algebra effectively, in contrast with many texts that present Boolean algebra and a few examples of its application and then leave it to the student to try to figure out how to use it effectively. For example, use of the theorem $x + yz = (x + y)(x + z)$ in factoring and multiplying out expressions is taught explicitly, and detailed guidelines are given for algebraic simplification.

Sequential circuits are given proper emphasis, with over half of the text devoted to this subject. The pedagogical strategy the text uses in teaching sequential circuits has proven to be very effective. The concepts of state, next state, etc. are first introduced for individual flip-flops, next for counters, then for sequential circuits with inputs, and finally for more abstract sequential circuit models. The use of timing charts, a subject neglected by many texts, is taught both because it is a practical tool widely used by logic design engineers and because it aids in the understanding of sequential circuit behavior.

The most important and often most difficult part of sequential circuit design is formulating the state table or graph from the problem statement, but most texts devote only a few paragraphs to this subject because there is no algorithm. This text devotes a full unit to the subject, presents guidelines for deriving state tables and graphs, and provides programmed exercises that help the student learn this material. Most of the material in the text is treated in a fairly conventional manner with the following exceptions:

(1) The diagonal form of the 5-variable Karnaugh map is introduced in Unit 5. (We find that students make fewer mistakes when using the diagonal form of 5-variable map in comparison with the side-by-side form.) Unit 5 also presents a simple algorithm for finding all essential prime implicants from a Karnaugh map.
(2) Both the state graph approach (Unit 18) and the SM chart approach (Unit 19) for designing sequential control circuits are presented.
(3) The introduction to the VHDL hardware description language in Units 10, 17, and 20 emphasizes the relation between the VHDL code and the actual hardware.

1.3 Using the Text in a Self-Paced Course

This section introduces the personalized system of self-paced instruction (PSI) and offers suggestions for using the text in a self-paced course. PSI (Personalized System of Instruction) is one of the most popular and successful systems used for self-paced instruction. The essential features of the PSI method are

(a) Students are permitted to pace themselves through the course at a rate commensurate with their ability and available time.
(b) A student must demonstrate mastery of each study unit before going onto the next.
(c) The written word is stressed; lectures, if used, are only for motivation and not for transmission of critical information.
(d) Use of proctors permits repeated testing, immediate scoring, and significant personal interaction with the students.

These factors work together to motivate students toward a high level of achievement in a well-designed PSI course.

The PSI method of instruction and its implementation are described in detail in the following references:

Keller, Fred S. and J. Gilmour Sherman, *The Keller Plan Handbook, W. A.* Benjamin, Inc., 1974.
Sherman, J.G., ed., *Personalized System of Instruction: 41 Germinal Papers, W. A.* Benjamin, Inc., 1974.

Results of applying PSI to a first course in logic design of digital systems are described in

Roth, C.H., "Continuing Effectiveness of Personalized Self-Paced Instruction in Digital Systems Engineering", *Engineering Education, Vol. 63, No. 6,* March 1973.

The instructor in charge of a self-paced course will serve as course manager in addition to his role in the classroom. For a small class, he may spend a good part of his time acting as proctor in the classroom, but as class size increases he will have to devote more of his time to supervision of course activities and less time to individual interaction with students. In his managerial role, the instructor is responsible for organizing the course, selection and training of proctors, supervision of proctors, and monitoring of student progress. The proctors play an important role in the success of

a self-paced course, and therefore their selection, training, and supervision is very important. After an initial session to discuss proper ways of grading readiness tests and interacting with students, weekly proctor meetings to discuss course procedures and problems may be appropriate.

A progress chart showing the units completed by each student is very helpful in monitoring student progress through the course. The instructor may wish to have individual conferences with students who fall too far behind. The instructor needs to be available in the classroom to answer individual student questions and to assist with grading of readiness tests as needed. He should make a special point to speak with the weak or slow students and give them a word of encouragement. From time to time he may need to settle differences which arise between proctors and students.

Various strategies for organizing a PSI course are described in the *Keller Plan Handbook*. The procedures that we use for operating our self-paced digital logic course are described in "Unit 0", which is available on the web: www.ece.utexas.edu/projects/ee316. At the first class meeting, we hand out a copy of Unit 0. The students are asked to read through Unit 0 and take a short test on the course procedures. This test is immediately evaluated so that the student can complete Unit 0 before the end of the first class period. In this way, the student is exposed to the basic way the course operates and is ready to proceed immediately with Unit 1 in the textbook.

During a typical class period, some of the students will spend their time studying but most of the students will come prepared to take a unit test. At the beginning of the period, the instructor or a proctor will be available to answer student questions on an individual basis. Later in the period, most of the time will be spent evaluating unit tests. We have found that a standard 50 minute class period is not long enough for a PSI session. We usually schedule sessions of 1½ or 2 hours or longer depending on class size. This allow adequate time for a student to have his questions answered, take a unit test, and have his test graded. Interactive grading of the tests with the student present is an important part of the PSI system and adequate time must be allowed for this activity. If you have a large number of students and proctors, you may wish to prepare a manual for guidance of your proctors. The procedures that we use for evaluating unit tests are described in a Proctor's Manual, which can be obtained by writing to Professor Charles H. Roth.

1.4. Use of Computer Software

Three software packages are included on the CD that accompanies the textbook. The first is a logic simulator program called *SimUaid*, the second is a basic computer-aided logic design program called *LogicAid*, and the third is a VHDL Simulator called *DirectVHDL*. In addition, we use the Xilinx ISE software for synthesizing VHDL code and downloading to CPLD or FPGA circuit boards. The Xilinx ISE software is available at nominal cost through the Xilinx University Program (for information, go to www.xilinx.com/univ/overview.html). A "Webpack" version of the Xilinx software is also available for downloading from the Xilinx.com website.

SimUaid provides an easy way for students to test their logic designs by simulating them. We first introduce *SimUaid* in Unit 4, where we ask the students to design a simple logic circuit such as problem 4.13 or 4.14, and simulate it. *SimUaid* is easy to learn, and it is highly interactive so that students can flip a simulated switch and immediately observe the result. In Unit 8, students design a multiple-output combinational logic circuit using NAND and NOR gates and test its operation using *SimUaid*. Students can use the simulator to help them understand the operation of latches and flip-flops in Unit 11. In Unit 12, we ask them to design a counter and simulate it (one part of problem 12.10). In Unit 16, students use *SimUaid* to test their sequential circuit designs. They can also generate VHDL code from their *SimUaid* circuit, synthesize it, and download it to a circuit board for hardware testing. In Unit 18, students can use the advanced features of *SimUaid* to simulate a multiplier or divider controlled by a state machine.

LogicAid provides an easy way to introduce students to the use of the computer in the logic design process. It enables them to solve larger, more practical design problems than they could by hand. They can also use *LogicAid* to verify solutions that they have worked out by hand. Instructors can use the program for grading homework and quizzes. We first introduce *LogicAid* in Unit 5. The program has a Karnaugh Map Tutorial mode that is very useful in teaching students to solve Karnaugh map problems. This tutorial mode helps students learn to derive minimum solutions from a Karnaugh map by informing them at each step whether that step is correct or not. It also forces them to choose essential prime implicants first. When in the KMap tutor mode, *LogicAid* prints "KMT" at the top of each output page, so you can check to see if the problems were actually solved in the tutorial mode.

Students can use *LogicAid* to help them solve design problems in Units 8, 16, 18, 19 and other units. For designing sequential circuits, they can input a state graph, convert it to a state table, reduce the state table, make a state assignment, and derive minimized logic equations for outputs and flip-flop inputs.

The *LogicAid* State Table Checker is useful for Units 14 and 16, and for other units in which students construct state tables. It allows students to check their solutions without revealing the correct answers. If the solution is wrong, the program displays a short input sequence for which the student's table fails. The *LogicAid* folder on the CD contains encoded copies of solutions for most of the state graph problems in *Fundamentals of Logic Design, 5th Ed.* If you wish to create a password-protected solution file for other state table problems, enter the state table into *LogicAid*, syntax check it, and then hold down the Ctrl key while you select Save As on the file menu. The Partial Graph Checker serves as a state graph tutor that allows a student to check his work at each step while constructing a state graph. If the student makes a mistake, it provides feedback so that the student can correct his answer. The partial graph checker works with any state graph problem for which an encoded state table solution file is provided.

The DirectVHDL simulator helps students learn VHDL syntax because it provides immediate visual feedback when they make mistakes. Our students use it for simulating VHDL code in Units 10, 17, and 20. Students can simulate and debug their code at home and then bring the code into lab for synthesis and hardware testing.

1.5. Suggested Equipment for Laboratory Exercises

Many types of logic lab equipment are available that are adequate to perform the lab exercises. Since most logic design is done today using programmable logic instead of individual ICs, we now recommend use of CPLDs or FPGAs for hardware implementation of logic circuit designs. At present, we are using the Digilab XCR Plus boards, which use a Xilinx Coolrunner XCR 3064 CPLD. This CPLD has an adequate number of logic cells to implement the lab exercises in the text. The board has 8 switches, 4 pushbuttons, 8 single LEDs, and two 7-segment LEDs.. The board also has a breadboard area. Information about this board and other CPLD and FPGA boards made by Digilent can be found on their website, www.digilentinc.com. We use the board in conjunction with the Xiliinx ISE software mentioned earlier.

II. SOLUTIONS TO HOMEWORK PROBLEMS
Unit 1 Problem Solutions

1.1 (a) 757.25_{10}

16 | 757		0.25
16 | 47	r5	16
16 | 2	r15=F_{16}	(4).00
0	r2	

$\therefore 757.25_{10} = 2F5.40_{16}$
$= \underline{0010}\ \underline{1111}\ \underline{0101}.\underline{0100}\ \underline{0000}_2$
2 F 5 4 0

1.1 (b) 123.17_{10}

16 | 123		0.17
16 | 7	r11	16
0	r7	(2).72
		16
		(11).52
		16
		(8).32

$\therefore 123.17_{10} = 7B.2B_{16}$
$= \underline{0111}\ \underline{1011}.\underline{0010}\ \underline{1011}_2$
7 B 2 B

1.1 (c) 356.89_{10}

16 | 356		0.89
16 | 22	r4	16
16 | 1	r6	(14).24
0	r1	16
		(3).84
		16
		(13).44
		16
		(7).04

$\therefore 356.89_{10} = 164.E3_{16}$
$= \underline{0001}\ \underline{0110}\ \underline{0100}.\underline{1110}\ \underline{0011}_2$
1 6 4 E 3

1.1 (d) 1063.5_{10}

16 | 1063		0.5
16 | 66	r7	16
16 | 4	r2	(8).00
0	r4	

$\therefore 1063.5_{10} = 427.8_{16}$
$= \underline{0100}\ \underline{0010}\ \underline{0111}.\underline{1000}_2$
4 2 7 8

1.2 (a) $EB1.6_{16} = E \times 16^2 + B \times 16^1 + 1 \times 16^0 + 6 \times 16^{-1}$
$= 14 \times 256 + 11 \times 16 + 1 + 6/16 = 3761.375_{10}$
$\underline{1110}\ \underline{1011}\ \underline{0001}.\underline{011(0)}_2$
E B 1 6

$7261.3_8 = 7 \times 8^3 + 2 \times 8^2 + 6 \times 8^1 + 1 + 3 \times 8^{-1}$
$= 7 \times 512 + 2 \times 64 + 6 \times 8 + 1 + 3/8 = 3761.375_{10}$
$\underline{111}\ \underline{010}\ \underline{110}\ \underline{001}.\underline{011}_8$
7 2 6 1 3

1.2(b) $59D.C_{16} = 5 \times 16^2 + 9 \times 16^1 + D \times 16^0 + C \times 16^{-1}$
$= 5 \times 256 + 9 \times 16 + 13 + 12/16 = 1437.75_{10}$
$\underline{0101}\ \underline{1001}\ \underline{1101}.\underline{1100}_{16}$
5 9 D C

$2635.6_8 = 2 \times 8^3 + 6 \times 8^2 + 3 \times 8^1 + 5 \times 8^0 + 6 \times 8^{-1}$
$= 2 \times 512 + 6 \times 64 + 3 \times 8 + 5 + 6/8 = 1437.75_{10}$
$\underline{010}\ \underline{110}\ \underline{011}\ \underline{101}.\underline{110}_8$
2 6 3 5 6

1.3 $3BA.25_{14} = 3 \times 14^2 + 11 \times 14^1 + 10 \times 14^0 + 2 \times 14^{-1} + 5 \times 14^{-2}$
$= 588 + 154 + 10 + 0.1684 = 752.1684_{10}$

6 | 752		0.1684
6 | 125	r2	6
6 | 20	r5	(1).0104
6 | 3	r2	6
0	r3	(0).0624
		6
		(0).3744
		6
		(2).2464
		6
		(1).4784

$\therefore 3BA.25_{14} = 752.1684_{10} = 3252.1002_6$

1.4 (a) 1457.11_{10}

16 | 1457		0.11
16 | 91	r1	16
16 | 5	r11=B_{16}	(1).76
0	r5	16
		(12).16

$\therefore 1457.11_{10} = 5B1.1C_{16}$

1.4 (b) $5B1.1C_{16} = \overbrace{5}\ \overbrace{B}\ \overbrace{1}\ \overbrace{1}\ \overbrace{C}$
$\overbrace{0101}\ \overbrace{1011}\ \overbrace{0001}.\overbrace{0001}\ \overbrace{1100}_2 = 2661.070_8$
2 6 6 1 0 7 0

1.4 (c) $5B1.1C_{16} = \underline{11}\ \underline{23}\ \underline{01}.\underline{01}\ \underline{30}_4$
5 B 1 1 C

1.4 (d) $DEC.A_{16} = D \times 16^2 + E \times 16^1 + C \times 16^0 + A \times 16^{-1}$
$= 3328 + 224 + 12 + 0.625 = 3564.625_{10}$

1.5 (a)

```
 111
 1111  (Add)      1111  (Sub)      1111  (Multiply)
+1010            -1010            ×1010
11001             0101             0000
                                  1111
                                  11110
                                 0000
                                 011110
                                1111
                                10010110
```

1.5 (b, c) *See FLD p. 625 for solution.*

1.6, 1.7, 1.8 *See FLD p. 625 for solution.*

1.10 (a) 1305.375_{10}

```
16 | 1305              0.375
16 | 81    r9          × 16
      5    r1         (6).000
```

$\therefore 1305.375_{10} = 519.600_{16}$

$= 0101\ 0001\ 1001.0110\ 0000\ 0000_2$ (5 1 9 6 0 0)

1.10 (b) 111.33_{10}

```
16 | 111                 0.33
      6   r15 = F16      × 16
                        (5).28
                         × 16
                        (4).48
```

$\therefore 111.33_{10} = 6F.54_{16}$

$= 0110\ 1111.0101\ 0100_2$ (6 F 5 4)

1.10 (c) 301.12_{10}

```
16 | 301             0.12
16 | 18   r13        × 16
      1   r2        (1).92
                     × 16
                   (14).72
```

$\therefore 301.12_{10} = 12D.1E_8$

$= 0001\ 0010\ 1101.0001\ 1110_2$ (1 2 D 1 E)

1.10 (d) 1644.875_{10}

```
16 | 1644              0.875
16 | 102   r12         × 16
      6    r6        (14).000
```

$\therefore 1644.875_{10} = 66C.E00_{16}$

$= 0110\ 0110\ 1100.1110\ 0000\ 0000_2$ (6 6 C E 0 0)

1.11 (a) $101\ 111\ 010\ 100.101_2 = 5724.5_8$

$= 5 \times 8^3 + 7 \times 8^2 + 2 \times 8^1 + 4 \times 8^0 + 5 \times 8^{-1}$

$= 5 \times 512 + 7 \times 64 + 2 \times 8 + 4 + 5/8$

$= 3028.625_{10}$

1.11 (b) $100\ 001\ 101\ 111.010_2 = 4157.2_8$

$= 4 \times 8^3 + 1 \times 8^2\ 5 \times 8^1 + 7 \times 8^0 + 2 \times 8^{-1}$

$= 4 \times 512 + 1 \times 64 + 5 \times 8 + 7 + 2/8$

$= 2159.25_{10}$

$1011\ 1101\ 0100.1010_2 = BD4.A_{16}$

$B \times 16^2 + D \times 16^1 + 4 \times 16^0 + A \times 16^{-1}$

$11 \times 256 + 13 \times 16 + 4 + 10/16$

$= 3028.625_{10}$

$1000\ 0110\ 1111.0100_2 = 86F.4_{16}$

$= 8 \times 16^2 + 6 \times 16^1 + F \times 16^0 \times 4 \times 16^{-1}$

$= 8 \times 256 + 6 \times 16 + 15 + 4/16$

$= 2159.25_{10}$

1.12 (a) $375.54_8 = 3 \times 64 + 7 \times 8 + 5 + 5/8 + 4/64 = 253.6875_{10}$

```
3 | 253          0.69
3 | 84   r1      ×  3
3 | 28   r0     (2).07
3 | 9    r1      ×  3
3 | 3    r0     (0).21
3 | 1    r0         3
    0    r1     (0).63
                    3
                (1).89
```

$\therefore 375.54_8 = 100101.2001_3$

1.12 (b) 384.74_{10}

```
4 | 384          0.74
4 | 96   r0      ×  4
4 | 24   r0     (2).96
4 | 6    r0      ×  4
4 | 1    r2     (3).84
    0    r1         4
                (3).36
```

$\therefore 384.74_{10} = 12000.233113_4 \ldots$

1.12 (c) $A52.A4_{11} = 10 \times 121 + 5 \times 11 + 2 + 10/11 + 4/121$
$= 1267.94_{10}$

9 | 1267		0.94
9 | 140	r7	9
9 | 15	r5	(8).46
9 | 1	r6	9
0	r1	(4).14

$\therefore A52.A4_{11} = 1267.94_{10} = 1657.8427_9...$

1.13 1110212.20211_3
01 11 02 12.20 21 10 = 1425.673_9

Base 3	Base 9
00	0
01	1
02	2
10	3
11	4
12	5
20	6
21	7
22	8

1.14 (a) $2983\ 63/64_{10}$ =

8 | 2983		0.984
8 | 372	r7	8
8 | 46	r4	(7).872
9 | 5	r6	8
0	r5	(6).976

$\therefore 2983\ 63/64_{10} = 5647.76_8$ (or 5647.77_8)
$= 101\ 110\ 100\ 111.111\ 110_2$
(or $101\ 110\ 100\ 111.111\ 111_{2)}$

1.14 (b) 93.70_{10}

8 | 93		0.70
8 | 11	r5	8
8 | 1	r3	(5).60
0	r1	8
		(4).80

$\therefore 93.70_{10} = 135.54_8 = 001\ 011\ 101.101\ 100_2$

1.14 (c) $1900\ 31/32_{10}$

8 | 1900		0.969
8 | 273	r4	8
8 | 29	r5	(7).752
9 | 3	r5	8
0	r3	(6).016

$\therefore 1900\ 31/32_{10} = 3554.76_8 = 011\ 101\ 101\ 100.111\ 110_2$

1.14 (d) 109.30_{10}

8 | 109		0.30
8 | 13	r5	8
8 | 1	r5	(2).40
0	r1	8
		(3).20

$\therefore 109.30_{10} = 155.23_8$
$= 001\ 101\ 101.010\ 011_2$

1.15(a)

```
 1 1 1          1 1 1
 1111 (Add)     1111 (Subtract)
 1001           1001
11000           0110
```

```
    1111 (Multiply)
    1001
    1111
   0000
   01111
  0000
 1 1 1
 001111
  1111
 10000111
```

1.15(b)

```
   1              1 1  1 1
 1101001 (Add)    1101001 (Sub)
  110110           110110
10011111          110011
```

```
    1101001  (Mult)
     110110
    0000000
   1101001
   11010010
  1101001
 1001110110
 0000000
 1 1 1
 1001110110
  1101001
 100100000110
 1101001
 1011000100110
```

1.15(c)

$$\begin{array}{r} {\scriptstyle 1}\\ 110010\\ 11101\\ \hline 1001111 \end{array}\ \text{(Add)} \qquad \begin{array}{r} {\scriptstyle 111\ 1}\\ 110010\\ 11101\\ \hline 10101 \end{array}\ \text{(Sub)} \qquad \begin{array}{r} 110010\\ 11101\\ \hline 110010\\ 000000\\ 0110010\\ 110010\\ \hline 1111010\\ 110010\\ \hline 1010001010\\ 110010\\ \hline 10110101010 \end{array}\ \text{(Mult)}$$

1.16(a)

$$\begin{array}{r} {\scriptstyle 1\ 1\ 1}\\ 10100100\\ 01110011\\ \hline 0110001 \end{array}$$

(b)

$$\begin{array}{r} {\scriptstyle 1\ \ 1}\\ 10010011\\ 01011001\\ \hline 00111010 \end{array}$$

(c)

$$\begin{array}{r} {\scriptstyle 11}\\ 11110011\\ 10011110\\ \hline 01010101 \end{array}$$

1.17(a)

```
      101110  Quotient
101 )11101001
     101
      1001
      101
       1000
       101
        110
        101
         11  Remainder
```

1.17(b)

```
      11011  Quotient
1110 )110000001
      1110
      10100
      1110
       11000
       1110
        10101
        1110
          111 Remainder
```

1.17(c)

```
      1100  Quotient
1001 )1110010
      1001
       1010
       1001
        110 Remainder
```

1.18 (a)

```
      10111  Quotient
110 )10001101
     110
      1011
      110
       1010
       110
        1001
        110
          11 Remainder
```

1.18(b)

```
      100011  Quotient
1011 )110000011
      1011
       10001
       1011
        1101
        1011
          10 Remainder
```

1.18(c)

```
      1011  Quotient
1010 )1110100
     1010
      10010
      1010
       10000
       1010
        110 Remainder
```

1.19

	4 3 2 1
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 1 0 0
4	1 0 0 0
5	1 0 0 1
6	1 0 1 0
7	1 1 0 0
8	1 1 0 1
9	1 1 1 0

9154 = 1110 0001 1001 1000

1.20 5-3-1-1 is possible, but 6-4-1-1 is not, because there is no way to represent 3 or 9.

Alternate Solutions:

	5 3 1 1	
0	0 0 0 0	
1	0 0 0 1	(0010)
2	0 0 1 1	
3	0 1 0 0	
4	0 1 0 1	(0110)
5	1 0 0 0	
6	1 0 0 1	(1010)
7	1 0 1 1	
8	1 1 0 0	
9	1 1 0 1	(1110)

1.21 5-4-1-1 is not possible, because there is no way to represent 3 or 8. 6-3-2-1 is possible:

	6 3 2 1
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 1 0 0
4	0 1 0 1
5	0 1 1 0
6	1 0 0 0
7	1 0 0 1
8	1 0 1 0
9	1 1 0 0

1.22 Alternate Solutions:

	6 2 2 1	
0	0 0 0 0	
1	0 0 0 1	
2	0 0 1 0	(0100)
3	0 0 1 1	(0101)
4	0 1 1 0	
5	0 1 1 1	
6	1 0 0 0	
7	1 0 0 1	
8	1 0 1 0	(1100)
9	1 0 1 1	(1101)

1100 0011 = 83

1.23 Alternate Solutions:

	5 2 2 1	
0	0 0 0 0	
1	0 0 0 1	
2	0 0 1 0	(0100)
3	0 0 1 1	(0101)
4	0 1 1 0	
5	1 0 0 0	
6	1 0 0 1	
7	1 0 1 0	(1100)
8	1 0 1 1	(1101)
9	1 1 1 0	

1110 0110 = 94

1.24 Alternate Solutions:

	7 3 2 1	
0	0 0 0 0	
1	0 0 0 1	
2	0 0 1 0	
3	0 1 0 0	(0011)
4	0 1 0 1	
5	0 1 1 0	
6	0 1 1 1	
7	1 0 0 0	
8	1 0 0 1	
9	1 0 1 0	
A	1 1 0 0	(1011)
B	1 1 0 1	

B4A9 = 1101 0101 1100 1010
Alt.: = " " 1011 "

1.25 (a) 222.22_{10}

16 | 222			0.22
16 | 13	r14		16
0	r13		(3).52
			16
			(8).32

$\therefore 222.22_{10} = DE.38_{16}$
$= \underline{1000100}\ \underline{1000101}\ \underline{0101110}\ \underline{0110011}\ \underline{0111000}$
D E . 3 8

1.25 (b) 183.81_{10}

16 | 183			0.81
16 | 11	r7		16
0	r11		(12).96
			16
			(15).36

$\therefore 183.81_{10} = B7.CF_{16}$
$= \underline{1000010}\ \underline{0110111}\ \underline{0101110}\ \underline{1000011}\ \underline{1000110}$
B 7 . C F

1.26 (a)

In 2's complement

(–10) + (–11)
110110
110101
(1)101011 (–21)

In 1's complement

(–10) + (–11)
110101
110100
1101001
1
101010 (–21)

1.26 (b)

In 2's complement

(–10) + (–6)
110110
11010
(1)110000 (–16)

In 1's complement

(–10) + (–6)
110101
111001
1101110
1
101111 (–16)

1.26 (c)

(–8) + (–11)
111000
110101
(1)101101 (–19)

(–8) + (–11)
110111
110100
1101011
1
101100 (–19)

1.26 (d)

11 + 9
001011
001001
010100 (20)

11 + 9
001011
001001
010100 (20)

1.26 (e)

(–11) + (–4)
110101
111100
(1)110001 (–15)

(–11) + (–4)
110100
111011
1101111
1
110000 (–15)

1.27 (a)

01001–11010

In 2's complement

01001
+ 00110
01111

In 1's complement

01001
+ 00101
01110

1.27 (b)

In 2's complement

11010
+ 00111
(1)00001

In 1's complement

11010
+ 00110
100000
1
00001

1.27 (c)

10110
+ 10011
(1)01001
overflow

10110
+ 10010
101000
1
01001
overflow

1.27 (d)

11011
+11001
(1)10100

11011
+11000
110011
1
10100

1.27 (e)

In 2's complement

11100
+ 01011
(1)00111

In 1's complement

11100
+ 01010
100110
1
00111

1.28 (a)

In 2's complement

11010
+ 01100
(1)00110

In 1's complement

11010
+ 01011
100101
1
00110

1.28 (b)

01011
+ 01000
10011

01011
+ 00111
10010

1.28 (c)

10001
+ 10110
(1)00111
overflow

10001
+ 10101
100110
1
00111
overflow

1.28 (d)

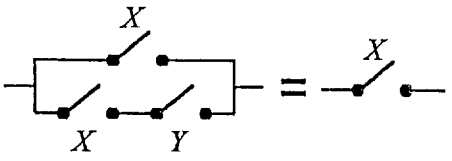
10101
+ 00110
11011

10101
+ 00101
11010

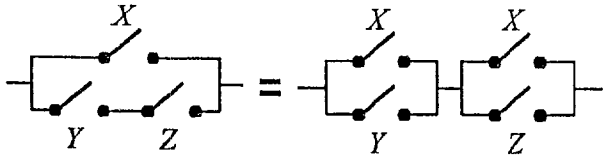
Unit 2 Problem Solutions

2.1 *See FLD p. 626 for solution.*

2.2 (a) In both cases, if X = 0, the transmission is 0, and if X = 1, the transmission is 1.



2.2 (b) In both cases, if X = 0, the transmission is YZ, and if X = 1, the transmission is 1.



2.3 *For the answer to 2.3, refer to FLD p. 626*

2.4 (a) $F = [(A \cdot 1) + (A \cdot 1)] + E + BCD = A + E + BCD$

2.4 (b) $Y = (AB' + (AB + B))\,B + A = (AB' + B)\,B + A$
$= (A + B)\,B + A = AB + B + A = A + B$

2.5 (a) $(A + B)\,(C + B)\,(D' + B)\,(ACD' + E)$
$= (AC + B)\,(D' + B)\,(ACD' + E)$ By Th. 8D
$= (ACD' + B)\,(ACD' + E)$ By Th. 8D
$= ACD' + BE$ By Th. 8D

2.5 (b) $(A' + B + C')\,(A' + C' + D)\,(B' + D')$
$= (A' + C' + BD)\,(B' + D')$
{By Th. 8D with $X = A' + C'$}
$= A'B' + B'C' + B'BD + A'D' + C'D' + BDD'$
$= A'B' + A'D' + C'B' + C'D'$

2.6 (a) $AB + C'D' = (AB + C')\,(AB + D')$
$= (A + C')\,(B + C')\,(A + D')\,(B + D')$

2.6 (b) $WX + WY'X + ZYX = X(W + WY' + ZY)$
$= X(W + ZY)$ {By Th. 10}
$= X(W + Z)\,(W + Y)$

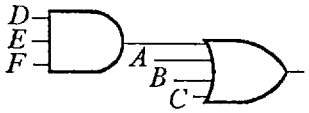
2.6 (c) $A'BC + EF + DEF' = A'BC + E(F + DF')$
$= A'BC + E(F + D) = (A'BC + E)\,(A'BC + F + D)$
$= (A' + E)\,(B + E)\,(C + E)\,(A' + F + D)$
$(B + F + D)\,(C + F + D)$

2.6 (d) $XYZ + W'Z + XQ'Z = Z(XY + W' + XQ')$
$= Z[W' + X(Y + Q')]$
$= Z(W' + X)\,(W' + Y + Q')$ By Th. 8D

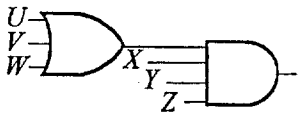
2.6 (e) $ACD' + C'D' + A'C = D'\,(AC + C') + A'C$
$= D'\,(A + C') + A'C$ By Th. 11D
$= (D' + A'C)\,(A + C' + A'C)$
$= (D' + A')\,(D' + C')\,(A + C' + A')$ By Th. 11D
$= (A' + D')\,(C + D')$

2.6 (f) $A + BC + DE = (A + BD + D)\,(A + BC + E)$
$= (A + B + D)\,(A + C + D)\,(A + B + E)$
$(A + C + E)$

2.7 (a) $\underline{(A + B + C} + D)\,\underline{(A + B + C} + E)\,\underline{(A + B + C} + F)$
$= \underline{A + B + C} + DEF$
Apply second distributive law (Th. 8D) twice



2.7 (b) $W\underline{XYZ} + V\underline{XYZ} + U\underline{XYZ} = \underline{XYZ}\,(W + V + U)$
By first distributive law (Th. 8)



2.8 (a) $[(AB)' + C'D]' = AB(C'D)' = AB(C + D')$
$= ABC + ABD'$

2.8 (b) $[A + B\,(C' + D)]' = A'(B(C' + D))'$
$= A'(B' + (C' + D)') = A'(B' + CD') = A'B' + A'CD'$

2.8 (c) $((A + B')\,C)'\,(A + B)\,(C + A)'$
$= (A'B + C')\,(A + B)C'A' = (A'B + C')A'BC'$
$= A'BC'$