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CHAPTER 3
MOS TRANSISTOR

3.1 Consider a MOS system with the following parameters:

- $t_{ox} = 200$ Å
- $\phi_{GC} = -0.85$ V
- $N_A = 2 \cdot 10^{15}$ cm^{-3}
- $Q_{ox} = q\, 2 \cdot 10^{11}$ C/cm^2

(a) Determine the threshold voltage V_{T0} under zero bias at room temperature (T=300K). Note that $\varepsilon_{ox} = 3.97\varepsilon_0$ and $\varepsilon_{si} = 11.7\varepsilon_0$.

(b) Determine the type (p-type or n-type) and amount of channel implant (N_I/cm^2) required to change the threshold voltage to 0.8V.

SOLUTION:

(a)

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$\phi_F = \frac{kT}{q} ln \frac{n_i}{N_A} = 0.026 ln \frac{1.45 \times 10^{10}}{2 \times 10^{15}} = -0.308 \text{ V}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.758 \times 10^{-7} \text{ F/cm}^2$$

$$\begin{aligned} Q_{B0} &= -\sqrt{2qN_A\varepsilon_{si}|-2\phi_F|} \\ &= -\sqrt{2 \cdot 1.6 \times 10^{-19} \cdot 2 \times 10^{15} \cdot 11.7 \times 8.854 \times 10^{-14} \cdot |-2 \times 0.308|} \\ &= -2.01 \times 10^{-8} \end{aligned}$$

$$V_{T0} = -0.85 + 0.615 + \frac{2 \times 10^{-8}}{1.758 \times 10^{-7}} - \frac{1.6 \times 10^{-19} \cdot 2 \times 10^{11}}{1.758 \times 10^{-7}} = -0.303 \text{ V}$$

(b) p-type implanted needed in the amount of:

$$\Delta V = 0.8 - V_{T0} = 0.8 + 0.303 = 1.303 = \frac{qN_I}{C_{ox}}$$

$$N_I = \frac{1.303 C_{ox}}{q} = \frac{1.303 \cdot 1.758 \times 10^{-7}}{1.6 \times 10^{-19}} = 1.21 \times 10^{12} \text{ cm}^{-2}$$

3.2 Consider a diffusion area which has the dimensions 10μm x 5μm and the abrupt junction depth is 0.5μm. Its n-type impurity doping level is $N_D = 1 \cdot 10^{20}$ cm^{-3} and the surrounding p-type substrate doping level is $N_A = 1 \cdot 10^{16}$ cm^{-3}. Determine the capacitance when the diffusion area is biased at 5V and the substrate is biased at 0V. In this problem, assume that there is no channel-stop implant.

SOLUTION:

$$C_j(V) = A \cdot \sqrt{\frac{\varepsilon_{si} \cdot q}{2} \left(\frac{N_A \cdot N_D}{N_A + N_D} \right)} \cdot \frac{1}{\sqrt{\phi_0 - V}}$$

$$\phi_0 = \frac{kT}{q} ln \frac{N_A \cdot N_D}{n_i^2} = 0.026 ln \frac{1 \times 10^{16} \cdot 1 \times 10^{20}}{\left(1.45 \times 10^{10}\right)^2} = 0.939$$

$$A = [5 \times 10 + 2(5 \times 0.5) + 2(10 \times 0.5)] = 65 \times 10^{-8}$$

$$C_j(V) = 65 \times 10^{-8} \sqrt{\frac{11.7 \cdot 8.854 \times 10^{-14} \cdot 1.6 \times 10^{-19}}{2} \left(\frac{1 \times 10^{36}}{1 \times 10^{20} + 1 \times 10^{16}} \right)} \frac{1}{\sqrt{0.939 + 5}}$$
$$= 7.678 \times 10^{-15} [F]$$

3.3 Describe the relationship between the mask channel length, L_M, and the electrical channel length, L. Are they identical? If not, how would you express L in terms of L_M and other parameters?

SOLUTION:

The electrical channel length is related to the mask channel length by:

$$L = L_M - 2L_D$$

where L_D is the lateral diffusion length.

3.4 How is the device junction temperature affected by the power dissipation of the chip and its package? Can you describe the relationship between the device junction temperature, ambient temperature, chip power dissipation and the packaging quality?

SOLUTION:

The device junction temperature at operating condition is given as $T_j = T_a + \Theta P_{diss}$, where T_a is the ambient temperature; P_{diss} is the power dissipated in the chip; Θ is the thermal resistance of the packaging. A cheap pakage will have high Θ which will result in large and possibly damaging junction temperature. Thus the choice of packaging must be such that it is both economic and pretective of the device.

3.5 Describe the three components of the load capacitance C_{load}, when a logic gate is driving other fanout gates.

SOLUTION:

The three major components of the load capacitance are interconnect capacitance, the next stage input capacitance, i.e., the gate capacitance and the drain parasitic capacitances of the current stage.

3.6 Consider a layout of an nMOS transistor shown in Fig.P3.6.
The process parameters are:
- $N_D = 2\cdot10^{20}\,cm^{-3}$
- $N_A = 1\cdot10^{15}\,cm^{-3}$
- $X_j = 0.5\ \mu m$
- $L_D = 0.5\ \mu m$
- $t_{ox} = 0.05\ \mu m$
- $V_{T0} = 0.8$ V
- Channel stop doping = 16.0 x (p-type substrate doping)

Find the effective drain parasitic capacitance when the drain node voltage changes from 5V to 2.5V.

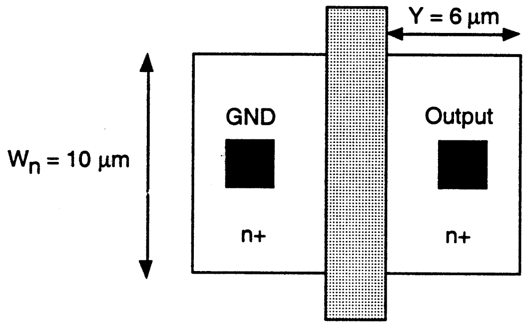


Figure P3.6

SOLUTION:

$$\phi_0 = \frac{kT}{q} ln \frac{N_A \cdot N_D}{n_i^2} = 0.026 ln\left[\frac{1\times10^{15}\cdot 2\times10^{20}}{\left(1.45\times10^{10}\right)^2}\right] = 0.8967[V]$$

$$\phi_{osw} = \frac{kT}{q} ln \frac{N_A' \cdot N_D}{n_i^2} = 0.026 ln\left[\frac{16\times10^{15}\cdot 2\times10^{20}}{\left(1.45\times10^{10}\right)^2}\right] = 0.9688[V]$$

$$C_{jo} = \sqrt{\frac{\varepsilon_{si}\cdot q}{2}\left(\frac{N_A\cdot N_D}{N_A+N_D}\right)}\cdot\frac{1}{\sqrt{\phi_o}}$$
$$= \sqrt{\frac{11.7\times8.854\times10^{-14}\times1.6\times10^{-19}\times10^{15}}{2\times0.8967}} = 9.6\times10^{-9}\left[F/cm^2\right]$$

$$C_{josw} = \sqrt{\frac{\varepsilon_{si} \cdot q}{2}\left(\frac{N_A' \cdot N_D}{N_A' + N_D}\right)} \cdot \frac{1}{\sqrt{\phi_{osw}}}$$

$$= \sqrt{\frac{11.7 \times 8.854 \times 10^{-14} \times 1.6 \times 10^{-19} \times 16 \times 10^{15}}{2 \times 0.9688}} = 36.94 \times 10^{-9} \left[F/cm^2\right]$$

$$C_{jsw} = X_j C_{josw} = 0.5 \times 10^{-4} \times 36.94 \times 10^{-9} = 1.847 [pF/cm]$$

$$A = Y \times W = 6 \times 10 = 60 \left[\mu m^2\right]$$

$$P = 2(Y + W) = 2(6 + 10) = 32 [\mu m]$$

$$K_{eq} = 2\sqrt{\phi_0}\left(\frac{\sqrt{\phi_0 + 5} - \sqrt{\phi_0 + 2.5}}{5 - 2.5}\right)$$

$$= 2\sqrt{0.8967}\left(\frac{\sqrt{5.8967} - \sqrt{3.3967}}{2.5}\right) = 0.44$$

$$K_{eq}' = 2\sqrt{\phi_{0sw}}\left(\frac{\sqrt{\phi_{0sw} + 5} - \sqrt{\phi_{0sw} + 2.5}}{5 - 2.5}\right)$$

$$= 2\sqrt{0.9688}\left(\frac{\sqrt{5.9688} - \sqrt{3.4688}}{2.5}\right) = 0.46$$

$$C_{drain} = K_{eq} \cdot C_{jo} \cdot A + K_{eq}' \cdot C_{jsw} \cdot P$$
$$= 0.44 \times 9.6 \times 10^{-9} \times 60 \times 10^{-8} + 0.46 \times 1.847 \times 10^{-12} \times 32 \times 10^{-4}$$
$$= 5.25 [fF]$$

3.7 A set of *I-V* characteristics of an nMOS transistor at room temperature are shown in below for different biasing conditions. Figure P3.7 shows the measurement setup. Using the data, find

(a) The threshold voltage V_{T0},
(b) electron mobility μ_n,
(c) body effect coefficient gamma(γ).

Some of the parameters are known to be:

- $W/L = 1.0$
- $t_{ox} = 345$ Å
- $|2\phi_F| = 0.64$ V

V_{GS}	V_{DS}	V_{SB}	I_D [μA]
4V	4V	0.0V	256
5V	5V	0.0V	441
4V	4V	2.6V	144
5V	5V	2.6V	256

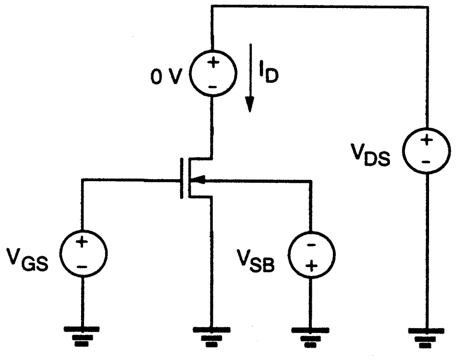


Figure P3.7

SOLUTION:

(a) Find V_{T0}
For both case 1 (Row1) and case 2(Row2), the transistor operates in saturation region, using equation (3.62)

$$I_D(sat) = \frac{k_n}{2}\left(V_{GS} - V_{T0}\right)^2$$

$$\frac{I_D(Row1)}{I_D(Row2)} = \frac{\left(4 - V_{T0}\right)^2}{\left(5 - V_{T0}\right)^2} = \frac{256}{441}.$$

$$\frac{4 - V_{T0}}{5 - V_{T0}} = \pm\frac{16}{21}$$

The correct solution is:

$$V_{T0} = 0.8[V]$$

(b) Find mobility

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{345 \times 10^{-8}} = 1.0 \times 10^{-7}[F/cm]$$

$$256 \times 10^{-6} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(4 - V_{T0})^2$$

$$\mu_n = \frac{2 \times 256 \times 10^{-6}}{1.0 \times 10^{-7} \times 1.0 \times 3.2^2} = 500\left[cm^2/V \cdot s\right]$$

(c) Find body effect coefficient γ
Using either Row 3 or Row4 data and equation (3.62), first find V_T

$$144 \times 10^{-6} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(4 - V_T)^2$$

$$V_T = 1.6[V]$$

from equation (3.64)

$$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}} = \frac{1.6 - 0.8}{\sqrt{0.64 + 2.6} - \sqrt{0.64}} = 0.8\left[V^{1/2}\right]$$

3.8 Compare the two technology scaling methods, namely, (i) the constant electric field scaling and (ii) the constant power supply voltage scaling. In particular, show analytically by using equations how the delay time, power dissipation, and power density are affected in terms of the scaling factor, S. To be more specific, what would happen if the design rules change from, say, 1μm to $1/S$ μm ($S > 1$)?

SOLUTION:

	$Const.\ E-field$	$Const.\ V_{DD}$
W, L, t_{ox}	$1/S$	$1/S$
V_{DD}	$1/S$	1
C_{ox}	S	S
$C \propto C_{ox}WL$	$1/S$	$1/S$
k_n, k_p	S	S
I_{DD}	$1/S$	S
$t_{delay} \propto \frac{C\Delta V}{I_{DD}}$	$1/S$	$1/S^2$
$Power \propto I_{DD}V_{DD}$	$1/S^2$	S
$Power\ density\left(\frac{Power}{Area}\right)$	1	S^3

3.9 A pMOS transistor was fabricated on a n-type substrate with a bulk doping density of $N_D = 10^{16}\ cm^{-3}$, gate doping density(n-type poly) of $N_D = 10^{20}\ cm^{-3}$, $Q_{ox}/q = 4\cdot 10^{10}\ cm^{-2}$ and gate oxide thickness of $t_{ox} = 0.1$ μm. Calculate the threshold voltage at room temperature for $V_{SB} = 0$. Use $\varepsilon_{si} = 11.7\varepsilon_0$.

SOLUTION:

$$\phi_F(substrate) = \frac{kT}{q} ln \frac{N_{D,sub}}{n_i} = 0.026\, ln \frac{1\times10^{16}}{1.45\times10^{10}} = 0.348[V]$$

$$\phi_F(gate) = \frac{kT}{q} ln \frac{N_{D,poly}}{n_i} = 0.026\, ln \frac{1\times10^{20}}{1.45\times10^{10}} = 0.587[V]$$

$$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate) = 0.348 - 0.587 = -0.239[V]$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\times8.85\times10^{-14}}{0.1\times10^{-4}} = 3.45\times10^{-8}\left[F/cm^2\right]$$

$$
\begin{aligned}
Q_{B0} &= \sqrt{2qN_{D,sub}\varepsilon_{si}|2\phi_F|} \\
&= \sqrt{2\times 1.6\times 10^{-19}\times 10^{16}\times 11.7\times 8.85\times 10^{-14}\times 2\times 0.348} \\
&= 4.8\times 10^{-8}\left[C/cm^2\right]
\end{aligned}
$$

$$
\begin{aligned}
V_{T0} &= \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \\
&= -0.239 - 2\times 0.348 - \frac{4.8\times 10^{-8}}{3.45\times 10^{-8}} - \frac{4\times 10^{10}\times 1.6\times 10^{-19}}{3.45\times 10^{-8}} \\
&= -2.51[V]
\end{aligned}
$$

3.10 A depletion-type nMOS transistor has the following device parameters:

- $\mu_n = 500$ cm²/V·s
- $t_{ox} = 345$ Å
- $|2\phi_F| = 0.84$ V
- $W/L = 1.0$

Some laboratory measurement results of terminal behavior of this device are shown in the table below. Using the data in the table, find the missing value of the gate voltage in the last entry. Show all of the details of your calculation.

$I_{DS}[\mu A]$	V_D	V_S	V_B	V_g
50.0	3V	0	0	0
40.0	5V	3V	0	?

SOLUTION:

Assume at case 1 (Row1), the transistor is saturated, therefore

$$
I_{ds} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs} - V_{T0}\right)^2 = \frac{1}{2}\times 500\times\frac{3.9\times 8.85\times 10^{-14}}{345\times 10^{-8}}\left(0 - V_{T0}\right)^2
$$

$$
V_{T0} = -1.41[V]
$$

This is consistant with the assumption.
Now find γ in order to find $V_T(V_{sb})$.
Since

$$
\phi_F = \frac{kT}{q}ln\frac{N_A}{n_i}
$$

$$
\frac{0.84}{2} = 0.026\,ln\frac{N_A}{1.45\times 10^{10}}
$$

$$
N_A = 1.6\times 10^{17}\left[cm^{-3}\right]
$$

From equation (3.24)

$$
\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}} = \frac{\sqrt{2\times 1.6\times 10^{-19}\times 1.6\times 10^{17}\times 11.7\times 8.85\times 10^{-14}}}{1.0\times 10^{-7}} = 2.3
$$

Note, γ is too large, this is a poorly designed device.

$$V_T(V_{sb}) = -1.41 + 2.3\times\left(\sqrt{3+0.84} - \sqrt{0.84}\right) = 0.99[V]$$

Using case 2 data, again, assuming the transistor is saturated,

$$40 = \frac{1}{2}\times 50\times\left(V_{gs} - 0.99\right)^2$$

$$V_{gs} = 2.25[V]$$

The assumption holds since,

$$V_{ds} = 2 > V_{gs} - V_T = 1.26$$

$$V_g = V_{gs} + V_s = 2.25 + 3 = 5.25[V]$$

3.11 Using the parameters given below, calculate the current through two nMOS transistors in series (see Fig. P3.11), when the drain of the top transistor is tied to V_{DD}, the source of the bottom transistor is tied to $V_{SS} = 0$ and their gates are tied to V_{DD}. The substrate is also tied to $V_{SS} = 0V$. Assume that $W/L = 10$ for both transistors.

- $k' = 25\ \mu A/V^2$
- $V_{TO} = 1.0$ V
- $\gamma = 0.39\ V^{1/2}$
- $|2\phi_F| = 0.6$ V

Hint: The solution requires some iterations and the body effect on threshold voltage has to be taken into account. Start with KCL equation.

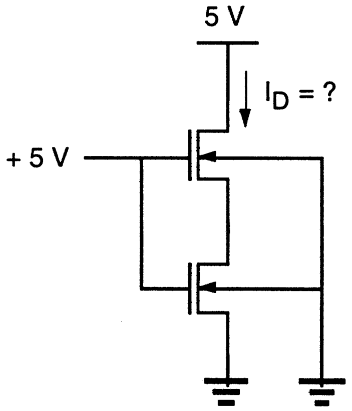


Figure P3.11

SOLUTION:

Since gate voltage is high, the midpoint V_x is expected to be low. Therefore, the load is in saturation and the driver is in linear region. From KCL

$$I_D = I_{D,driver} = I_{D,load}$$

$$\frac{1}{2}k'\frac{W}{L}\left(5 - V_x - V_{T,L}(V_x)\right)^2 = \frac{1}{2}k'\frac{W}{L}\left(2(5 - V_{TO})V_x - V_x^2\right)$$

Using the following two equation to iteratively find the solution.

$$\begin{cases} \left(5 - V_x - V_{T,L}(V_x)\right)^2 = 8V_x - V_x^2 \\ V_{T,L}(V_x) = 1 + 0.39\left(\sqrt{0.6 + V_x} - \sqrt{0.6}\right) \end{cases}$$

The intermediate values are listed in the table:

$V_{T,L}(V_x)$	V_x
1	2.83
1.42	0.97
1.19	1.08
1.20	1.07
1.20	1.07

$$I_D = \frac{1}{2}k'\frac{W}{L}\left(8V_x - V_x^2\right) = 0.5\times25\times10\times\left(8\times1.07 - 1.07^2\right) = 927[\mu A]$$

3.12 The following parameters are given for an nMOS process.

- $t_{ox} = 500\text{Å}$
- substrate doping $N_A = 1\cdot10^{16}\,\text{cm}^{-3}$
- polysilicon gate doping $N_D = 1\cdot10^{20}\,\text{cm}^{-3}$
- oxide-interface fixed-charge density $N_{ox} = 2\cdot10^{10}\,\text{cm}^{-3}$

(a) Calculate V_T for an unimplanted transistor.

(b) What type and what concentration of impurities must be implanted to achieve V_T = +2V and V_T = -2V?

SOLUTION:

(a) For unimplanted transistor,

$$\phi_F(substrate) = \frac{kT}{q}ln\frac{n_i}{N_A} = 0.026\,ln\frac{1.45\times10^{10}}{1.0\times10^{16}} = -0.35[V]$$

$$\phi_F(gate) = \frac{kT}{q}ln\frac{N_{D,poly}}{n_i} = 0.026\,ln\frac{1\times10^{20}}{1.45\times10^{10}} = 0.59[V]$$

$$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate) = -0.35 - 0.59 = -0.94[V]$$

$$\begin{aligned} Q_{B0} &= \sqrt{2qN_{A,sub}\varepsilon_{si}|2\phi_F|} \\ &= \sqrt{2\times1.6\times10^{-19}\times10^{16}\times11.7\times8.85\times10^{-14}\times2\times0.35} \\ &= -4.82\times10^{-8}\left[C/cm^2\right] \end{aligned}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\times8.85\times10^{-14}}{500\times10^{-8}} = 6.9\times10^{-8}\left[F/cm^2\right]$$

$$V_{T0}=\Phi_{GC}-2\phi_F-\frac{Q_{B0}}{C_{ox}}-\frac{Q_{ox}}{C_{ox}}$$
$$=-0.94-2\times(-0.35)-\frac{\left(-4.82\times10^{-8}\right)}{6.9\times10^{-8}}-\frac{2\times10^{10}\times1.6\times10^{-19}}{6.9\times10^{-8}}$$
$$=0.41[V]$$

(b) For $V_T=2V$:

$$V_T=2=V_{T0}-\frac{Q_{II}}{C_{ox}}=0.412-\frac{Q_{II}}{C_{ox}}$$

Negative charges needed in this case, so it must be p-type implant in the amount of $Q_{II}=qN_I=(V_T-V_{T0})C_{ox}$

$$N_I=(2-0.41)\times\frac{6.9\times10^{-8}}{1.6\times10^{-19}}=6.85\times10^{11}\left[cm^{-3}\right]$$

For $V_T=-2V$,positive charges need, must be n-type implant,

$$N_I=(2+0.41)\times\frac{6.9\times10^{-8}}{1.6\times10^{-19}}=1.04\times10^{12}\left[cm^{-3}\right]$$

3.13 Using the measured data given below, determine the device paramenters V_{T0}, k, γ, and λ, assuming $2\phi_F=-0.6$ V.

V_{GS}	V_{DS}	V_{BS}	I_D[µA]
2	5	0	10
5	5	0	400
5	5	-3	280
5	8	0	480

SOLUTION:

When $V_{DS}\ge V_{GS}$, the transistor operates in saturation region, therefore

$$I_{DSAT}=\frac{k}{2}\left(V_{GS}-V_T\right)^2\left(1+\lambda V_{DS}\right)$$

a) Find λ:

$$\frac{I_{DSAT}(Row4)}{I_{DSAT}(Row2)}=\frac{1+\lambda V_{DS}(Row4)}{1+\lambda V_{DS}(Row2)}=\frac{1+8\lambda}{1+5\lambda}=\frac{480}{400}$$
$$\lambda=0.1\left[V^{-1}\right]$$

b) Find V_{T0}

$$\frac{I_{DSAT}(Row2)}{I_{DSAT}(Row1)}=\frac{\left(5-V_{T0}\right)^2}{\left(2-V_{T0}\right)^2}$$
$$V_{T0}=1.44[V]\quad and\quad V_{T0}=2.41[V](unreal)$$

c) Find k:
From Row2 data,

$$400 = \frac{k}{2}(5-1.44)^2(1+0.1\times 5)$$

$$k = 42\left[\mu A / V^2\right]$$

d) Find γ:
From Row3 data,

$$280 = \frac{42}{2}\left(5 - V_T\left(V_{BS} = -3\right)\right)^2(1+0.1\times 5)$$

$$V_T\left(V_{BS} = -3\right) = 2.02[V]$$

$$2.02 = 1.44 + \gamma\left(\sqrt{3+0.6} - \sqrt{0.6}\right)$$

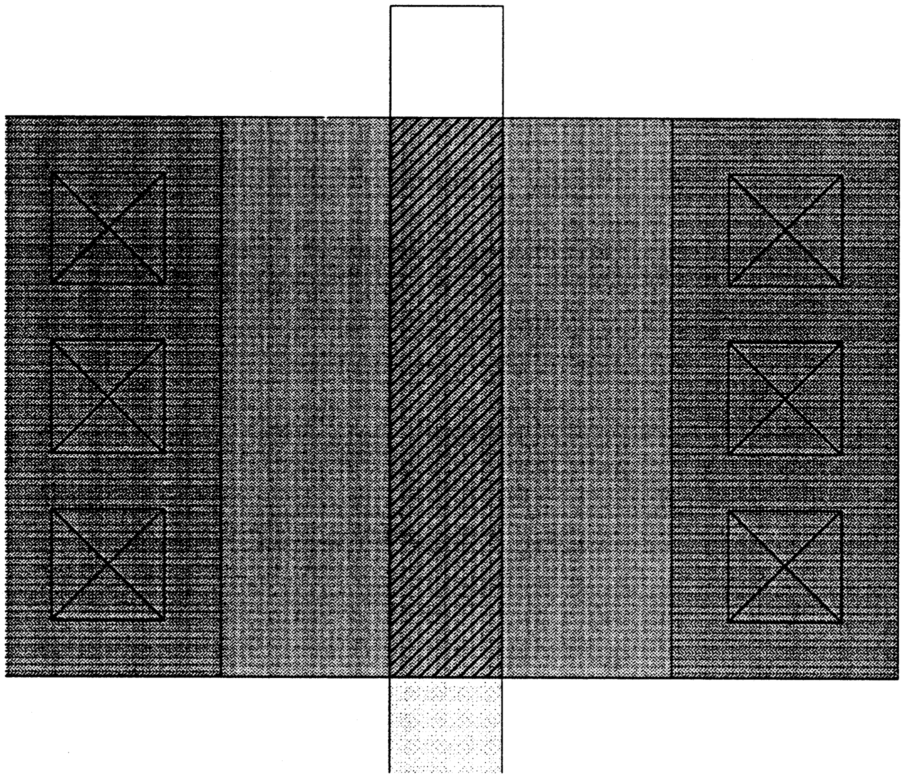
$$\gamma = 0.52\left[V^{1/2}\right]$$

3.14 Using the design rules specified in Chapter 2, sketch a simple layout of an nMOS transistor on grid paper. Use a minimum feature size of 3µm. Neglect the substrate connection. After you complete the layout, calculate approximate values for C_g, C_{sb}, and C_{db}. The following parameters are given:

- Substrate doping $N_A = 10^{16}$ cm^{-3}
- Drain/source doping $N_D = 10^{19}$ cm^{-3}
- $W = 15$ µm
- $L = 3$ µm
- $t_{ox} = 0.05$ µm

SOLUTION:

The layout is shown in the following.



Calculate capacitances:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{500 \times 10^{-8}} = 6.9 \times 10^{-8}\ \mathrm{F/cm^2}$$

$$C_g = C_{ox}WL = 6.9 \times 10^{-8} \times 15 \times 3 \times 10^{-8} = 31.5\ \mathrm{fF}$$

Since drain and source have the same geometry, the junction capacitance are the same.

$$\phi_0 = \frac{kT}{q} ln \frac{N_A \cdot N_D}{n_i^2} = 0.026 ln \left[\frac{1 \times 10^{16} \cdot 1 \times 10^{19}}{\left(1.45 \times 10^{10}\right)^2} \right] = 0.879\ \mathrm{V}$$

$$\phi_{osw} = \frac{kT}{q} ln \frac{N_A(sw) \cdot N_D}{n_i^2} = 0.026 ln \left[\frac{1 \times 10^{17} \cdot 1 \times 10^{19}}{\left(1.45 \times 10^{10}\right)^2} \right] = 0.939\ \mathrm{V}$$

$$C_{jo} = \sqrt{\frac{\varepsilon_{si} \cdot q}{2}\left(\frac{N_A \cdot N_D}{N_A + N_D}\right)} \cdot \frac{1}{\sqrt{\phi_o}}$$

$$= \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19} \times 10^{16}}{2 \times 0.879}} = 3.07 \times 10^{-8}\ \mathrm{F/cm^2}$$

$$C_{josw} = \sqrt{\frac{\varepsilon_{si} \cdot q}{2}\left(\frac{N_A(sw) \cdot N_D}{N_A(sw) + N_D}\right)} \cdot \frac{1}{\sqrt{\phi_{osw}}}$$

$$= \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19} \times 1 \times 10^{17}}{2 \times 1.01 \times 0.939}} = 9.35 \times 10^{-8}\ \mathrm{F/cm^2}$$

Assume junction depth is 0.5μm,

$$C_{jsw} = X_j C_{josw} = 0.5 \times 10^{-4} \times 9.35 \times 10^{-8} = 4.67\ \mathrm{pF/cm}$$

$$AD = AS = Y \cdot W = 10.5 \times 15 = 157.5\ \mu\mathrm{m}^2$$

$$PD = PS = 2(Y + W) = 51\ \mu\mathrm{m}$$

$$\begin{aligned} C_{db} = C_{sb} &= AD \cdot C_{jo} + PD \cdot C_{jsw} \\ &= 157.5 \times 10^{-8} \times 3.07 \times 10^{-8} + 51 \times 10^{-4} \times 4.67 \times 10^{-12} \\ &= 72.2\ \mathrm{fF} \end{aligned}$$

3.15 Derive the current equation for a p-channel MOS transistor operating in the linear region, i.e., for $V_{SG}+V_{TP}>V_{SD}$.

SOLUTION:

Following the analysis in the text, section 3.4, using gradual channel approximation:

$$Q_I(y) = C_{ox}(V_{SG} - V_C(y) - V_{TP})$$

$$dR = \frac{dy}{W \cdot \mu_p \cdot Q_I(y)}$$

$$dV_C = I_D \cdot dR = \frac{I_D}{W \cdot \mu_p \cdot Q_I(y)} dy$$

$$\int_0^L I_D dy = W \cdot \mu_p \int_0^{V_{SD}} Q_I \cdot dV_C$$

$$I_D \cdot L = W \cdot \mu_p \cdot C_{ox} \int_0^{V_{SD}} \left(V_{SG} - V_c(y) - V_{TP}\right) \cdot dV_C$$

$$I_D = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L}\left[2(V_{SG} - V_{TP})V_{SD} - V_{SD}^2\right]$$

3.16 An enhancement-type nMOS transistor has the following parameters:

- $V_{T0} = 0.8\text{V}$
- $\gamma = 0.2\text{V}^{1/2}$
- $\lambda = 0.05\text{V}^{-1}$
- $|2\phi_F| = 0.58\text{V}$
- $k' = 20\ \mu\text{A/V}^2$

(a) When the transistor is biased with $V_G = 2.8$ V, $V_D = 5$ V, $V_S = 1$ V, $V_B = 0$ V, the drain current $I_D = 0.24$ mA. Determine W/L.
(b) Calculate I_D for $V_G = 5$ V, $V_D = 4$ V, $V_S = 2$ V and $V_B = 0$ V.
(c) If $\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s}$ and $C_g = C_{ox}\cdot W\cdot L = 1.0\text{x}10^{-15}$ F, find W and L.

SOLUTION:

(a) For enhancement transistor and $V_{T0} > 0$, it must be nMOS.

$$V_T(V_{SB}) = V_{T0} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right)$$
$$= 0.8 + 0.2\cdot\left(\sqrt{0.58+1} - \sqrt{0.58}\right) = 0.899[V]$$
$$\because V_{DS} = 4 > V_{GS} - V_T = 1.8 - 0.899 = 0.901$$

nMOS transistor is in saturation region.

$$\because I_D(sat) = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$
$$\therefore \frac{W}{L} = \frac{2\cdot I_D(sat)}{k'\cdot(V_{GS} - V_T)^2(1 + \lambda V_{DS})}$$
$$= \frac{2\cdot 0.24\times 10^{-3}}{20\times 10^{-6}(1.8 - 0.899)^2(1 + 0.05\times 4)} = 24.64$$

(b)

$$V_T(V_{SB}) = V_{T0} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right)$$
$$= 0.8 + 0.2\cdot\left(\sqrt{0.58+2} - \sqrt{0.58}\right) = 0.969[V]$$
$$\because V_{DS} = 2 < V_{GS} - V_T = 3 - 0.969 = 2.031$$

nMOS transistor is in linear region.

$$I_D(lin) = \frac{k'}{2}\frac{W}{L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]\left[1 + \lambda V_{DS}\right]$$
$$= 10\times 10^{-6}\times 24.64\left[2\times(3 - 0.969)\times 2 - 4\right]\left[1 + 0.05\times 2\right]$$
$$= 1.12[mA]$$

(c)

$$C_{ox} = \frac{k'}{\mu_n} = \frac{20\times 10^{-6}}{500} = 4\times 10^{-8}\left[F/cm^2\right]$$

$$\begin{cases} W \cdot L = \dfrac{C_g}{C_{ox}} = \dfrac{10^{-15}}{4\times10^{-8}} = 2.5\times10^{-8}\left[cm^2\right] \\ \dfrac{W}{L} = 24.64 \end{cases}$$

Solve for W and L,

$$\begin{cases} W = 7.85[\mu m] \\ L = 0.32[\mu m] \end{cases}$$

3.17 An nMOS transistor is fabricated with the following physical parameters:

- $N_D = 10^{20}\,cm^{-3}$
- N_A(substrate) $= 10^{16}\,cm^{-3}$
- N^+_A(chanstop) $= 10^{19}\,cm^{-3}$
- $W = 10\ \mu m$
- $Y = 5\ \mu m$
- $L = 1.5\ \mu m$
- $L_D = 0.25\ \mu m$
- $X_j = 0.4\ \mu m$

(a) Determine the drain diffusion capacitance for $V_{DB} = 5$ V and 2.5V.

(b) Calculate the overlap capacitance between the gate and drain for an oxide thickness of $t_{ox} = 200$ Å.

SOLUTION:

(a)

$$\phi_o = \frac{kT}{q} ln\frac{N_A N_D}{n_i^2} = 0.026\, ln\frac{10^{16}\cdot10^{20}}{\left(1.45\times10^{10}\right)^2} = 0.94[V]$$

$$\begin{aligned} C_{jo} &= \sqrt{\frac{\varepsilon_{si}\cdot q}{2}\left(\frac{N_A\cdot N_D}{N_A+N_D}\right)\cdot\frac{1}{\phi_o}} \\ &= \sqrt{\frac{11.7\times8.85\times10^{-14}\times1.6\times10^{-19}}{2}\cdot\frac{10^{20}\cdot10^{16}}{10^{20}+10^{16}}\cdot\frac{1}{0.94}} \\ &= 2.98\times10^{-8}\left[F/cm^2\right] \end{aligned}$$

$$A = W\cdot Y + W\cdot X_j = 10\times5 + 10\times0.4 = 54\left[\mu m^2\right]$$

$$C_j(V) = \frac{A\cdot C_{jo}}{\sqrt{1-\dfrac{V}{\phi_o}}}$$

$$C_j(-5)=\frac{54\times10^{-8}\cdot2.98\times10^{-8}}{\sqrt{1+\frac{5}{0.94}}}=6.4\times10^{-15}[F]$$

$$C_j(-2.5)=\frac{54\times10^{-8}\cdot2.98\times10^{-8}}{\sqrt{1+\frac{2.5}{0.94}}}=8.41\times10^{-15}[F]$$

For sidewall capacitance calculation,

$$\phi_{osw}=\frac{kT}{q}ln\frac{N_A(sw)\cdot N_D}{n_i^2}=0.026ln\frac{10^{19}\cdot10^{20}}{\left(1.45\times10^{10}\right)^2}=1.118[V]$$

$$C_{josw}=\sqrt{\frac{\varepsilon_{si}\cdot q}{2}\left(\frac{N_A(sw)\cdot N_D}{N_A(sw)+N_D}\right)\cdot\frac{1}{\phi_{osw}}}$$
$$=\sqrt{\frac{11.7\times8.85\times10^{-14}\times1.6\times10^{-19}}{2}\cdot\frac{10^{20}\cdot10^{19}}{10^{20}+10^{19}}\cdot\frac{1}{1.118}}$$
$$=8.207\times10^{-7}\left[F/cm^2\right]$$

$$C_{jsw}(V)=\frac{P\cdot X_j\cdot C_{josw}}{\sqrt{1-\frac{V}{\phi_{osw}}}}=\frac{(2\times5+10)\times0.4\times8.207\times10^{-7}}{\sqrt{1-\frac{V}{\phi_{osw}}}}$$
$$=\frac{6.566\times10^{-14}}{\sqrt{1-\frac{V}{\phi_{osw}}}}[F]$$

$$C_{jsw}(-5V)=\frac{6.566\times10^{-14}}{\sqrt{1+\frac{5}{1.118}}}=28.07\times10^{-15}[F]$$

$$C_{jsw}(-2.5V)=\frac{6.566\times10^{-14}}{\sqrt{1+\frac{2.5}{1.118}}}=36.50\times10^{-15}[F]$$

$$\langle C_{db}\rangle(-5V)=C_j(-5V)+C_{jsw}(-5V)=6.4+28.07=34.47[fF]$$
$$\langle C_{db}\rangle(-2.5V)=C_j(-2.5V)+C_{jsw}(-2.5V)=8.41+36.5=44.91[fF]$$

(b)

$$C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}=\frac{3.9\times8.85\times10^{-14}}{200\times10^{-8}}=1.726\times10^{-7}\left[F/cm^2\right]$$

$$C_{gd}=C_{ox}\cdot W\cdot L_D=1.726\times10^{-7}\times10\times10^{-4}\times0.25\times10^{-4}=4.31[fF]$$