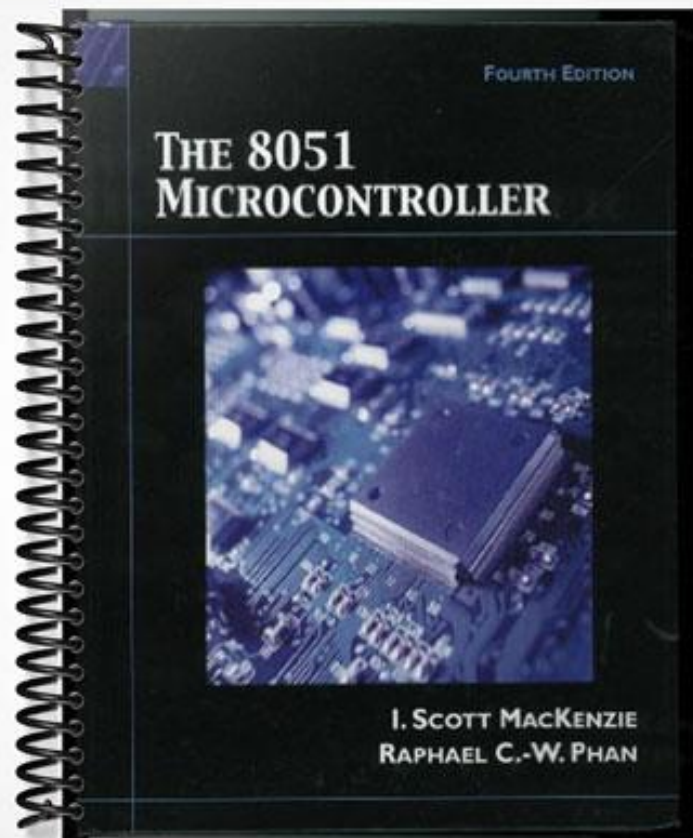
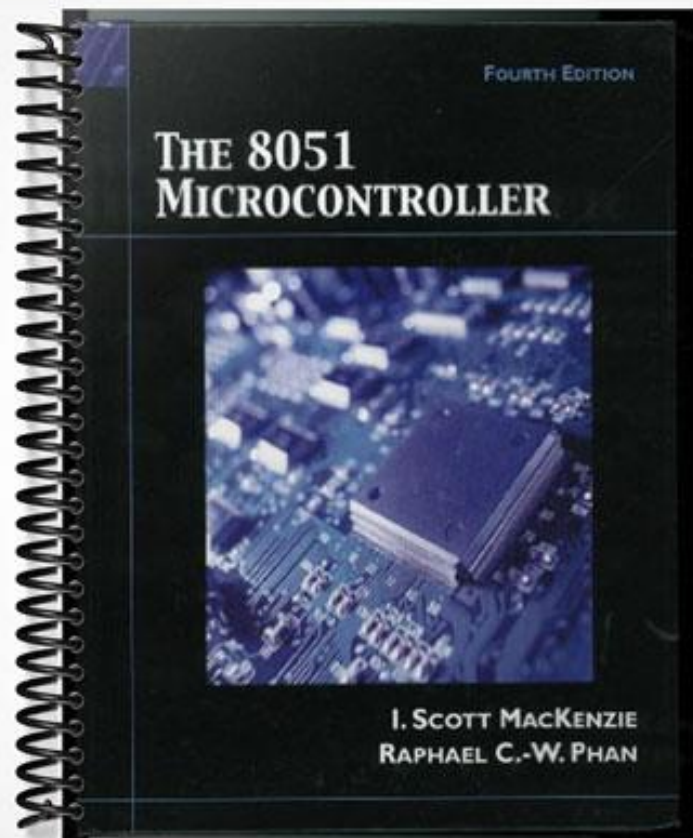


SOLUTIONS MANUAL



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Instructor's Manual and PowerPoints

to accompany

THE 8051 MICROCONTROLLER

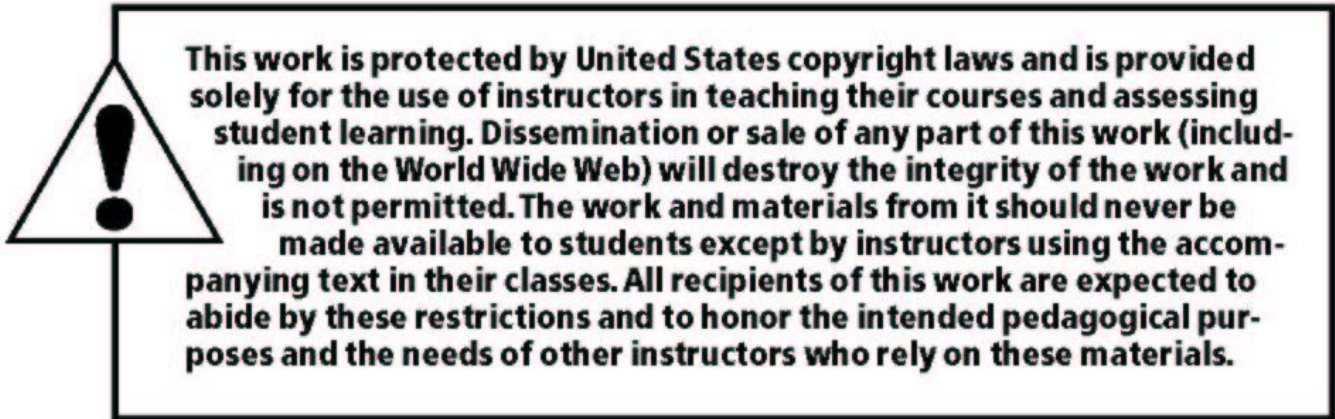
Fourth Edition

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THE 8051 MICROCONTROLLER

Fourth Edition

Instructor's Manual

This manual contains solutions to the problems at the end of the chapters in The 8051 Microcontroller (4th edition). Additional materials are provided that should prove useful for instructors delivering a lecture + lab course on the 8051 microcontroller. These include the following:

- Discussions on the solutions
- Laboratory project suggestions

Discussions on solutions are provided to assist instructors in discussing with students the solutions to problems.

Laboratory project suggestions are provided with selected problems which lend themselves to further exploration in a laboratory setting. Instructors may wish to distribute the initial solution (given in this manual) to assist students in getting started. Extensions to the basic problem are given in the form of defined tasks to be solved using software and/or hardware. The tasks are defined in a manner that facilitates demonstration in the laboratory.

Courses based on the 8051 will require a single-board computer for laboratory projects. Although many 8051 SBCs are available (sources are provided in Appendix H in the text), the SBC-51 described in Chapter 10 is a logical choice for the initial laboratory project. A section is provided at the end of this manual to facilitate construction and testing of the SBC-51.

This solutions manual has been updated with a total of 72 new questions have been added, for a total of 200.

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August 2003

Chapter 1 - Introduction to Microcontrollers

1.
 - (a) The first widely used microprocessor was the 8080.
 - (b) The 8080 was introduced in 1970 by Intel Corp.
2. MOS Technology was responsible for the 6502 microprocessor, Zilog for the Z80.
3.
 - (a) The 8051 was introduced in 1980.
 - (b) The predecessor of the 8051 was the 8048, introduced in 1976.
4.
 - (a) RAM (random access memory) and ROM (read-only memory).
 - (b) ROM retains its contents even when powered-off.
 - (c) The term "non-volatile" describes this property of ROM.
5.
 - (a) The program counter
 - (b) The program counter contains the address of the next instruction to be executed.
6.
 - (a) The address bus contains the content of the program counter. The data bus contains the opcode of the instruction.
 - (b) The information on the address bus is output, originating from the CPU. The information on the data bus is input, originating from the RAM.
7. $2^{18} = 2^8 \times 2^{10} = 256\text{K}$ bytes.
8. The phrase "16-bit computer" refers to a computer system with 16 lines on its data bus.
9. Online storage is directly accessible through software, whereas archival storage is "off-line" and must be loaded onto a system by a human operator before it can be accessed by software.
10. Optical disks are also used for archival storage.
11. Human factors is a field of engineering which seeks to match the characteristics of people with (computing) machines, to achieve a safe, comfortable, and efficient working environment.
12. Input devices: joystick, light pen, mouse, and microphone
Output device: loudspeaker
13.
 - (a) The lowest level of software is the input/output subroutines.
 - (b) These subroutines directly access to the system's hardware for input/output operations.

14.
 - (a) An actuator is an output device, whereas a sensor is an input device.
 - (b) A relay is an actuator, a thermistor is a sensor.

15.
 - (a) Firmware is software stored in ROM or EPROM.
 - (b) Microcontrollers rely more heavily on firmware than microprocessors.
 - (c) Microcontrollers usually have only a small amount of RAM and they lack a disk drive from which to load programs into RAM.

16. Microcontrollers include instructions to operate on and manipulate bits. These bits are sometimes 1-bit I/O ports on the microcontroller chip that are directly addressable through simple instructions.

17. Five possible products that are likely to use microcontrollers include a hand-held video game, a telephone answering machine, an electronic fish finder, a remote-controlled toy car, and a video camera.

Chapter 2 - Hardware Summary

1. Fujitsu, Siemens, Advanced Micro Devices, Philips
2. The most likely choice is the 8052 because it includes 8K bytes of on-chip ROM.

3.

```
SETB    28H
```

The bit address is found in Figure 2-6 in the text. The figure shows the relationship between addressable bits and the byte addresses where the bits are located.

4.

```
MOV     C,00H
ORL     C,01H
MOV     02H,C
```

All logical operations on bits must use the carry flag — the Boolean accumulator — as one of the bits in the operation. An initial "MOV C,bit" instruction is usually necessary before the logical operation can be performed. The result must be written to the destination address using a "MOV bit,C" instruction.

5.

```
MOV     C,P0.0
MOV     P3.0,C
```

6.

```
MOV     C,P1.0
ANL     C,P1.1
MOV     P3.0,C
```

7.

```
MOV     C,P1.0
JNB     P1,1,SKIP
CPL     C
SKIP:   MOV     P3.0,C
```

8.

```
MOV     C,P1.0
ORL     C,P1.1
CPL     C
MOV     P3.0,C
```


9.

For Problem 6:



For Problem 7:



For Problem 8:



10. (a) bits 31H, 32H, 35H
(b) bits 31H, 33H, 34H-36H
(c) bits E0H, E1H, E4H, DOH (Note: P bit in PSW set)
(d) bits 78H-7FH
(e) bit 91H
(f) bits B2H, B3H]

11.

```
MOV     A, #55H
```

12.

```
MOV     A, #0ABH
MOV     DPTR, #9A00H
MOV     @DPTR, A
```

13. 26

14. 07H (see Table 2-6)

15. (a)

```
MOV     SP, #3FH
```

(b)

```
MOV     SP, #0BFH
```

16. (a)

```
MOV     SP, #5FH
```

(b)

```
MOV     SP, #0DFH
```

17.

```
SUB:    PUSH    PSW            ;save previous status
        SETB   RS0            ;enable register bank 3
        SETB   RS1            ; RS0 = RS1 = 1
        ...                   ;execute subroutine
        POP    PSW            ;restore previous status
        RET                               ;return to main program
```

The subroutine is given the name "SUB". "PSW" is a pre-defined assembler symbol equivalent to "0D0H" (see Figure 2-2); so, PUSH PSW is the same as

```
PUSH    0D0H
```

The PUSH and POP instructions only exist in the following forms:

```
PUSH    direct
POP     direct
```

So, registers can only be pushed on the stack or popped from the stack using the corresponding direct address or, as illustrated in this example, the equivalent pre-defined assembler symbol.

The SETB instructions could be replaced with

```
MOV     PSW, #30H
```

which, in a single instruction, sets the RS0 and RS1 bits, thus activating register bank 3. The savings is one byte (3 bytes vs. 4 bytes); so, the latter method, despite being less "readable", may be preferred if conserving code memory is important.

18. (a) register bank 3
(b) register bank 1
(c) register bank 1

19. (a) register bank 1
(b) register bank 0
(c) register bank 2

20. 2.67 MHz

The "cycle" frequency of the 8051 is one twelfth the crystal frequency. However, ALE pulses twice per cycle (see Figure 2-9); therefore, the ALE frequency is one sixth the crystal frequency, or

$$16 / 6 = 2.67 \text{ MHz}$$

21. 3 μ s

A machine cycle lasts twelve periods of the crystal clock. At 4 MHz, this is $1/4 \times 12 \mu$ s = 3 μ s.

22. 1.67 MHz

ALE pulses twice per machine cycle, or once every 6 periods of the crystal clock. At 10 MHz, ALE pulses every $1/10 \times 6 = 0.6 \mu$ s, for a frequency of $10/6 = 1.67$ MHz.

23. 0.33 or 33%

As seen in Figure 2-9, ALE is high for four of the twelve phases in a machine cycle. $4/12 = 0.33$.

24. (a) 3.0 μ s

At 8 MHz, a machine cycle lasts $1/8 \times 12 \mu$ s = 1.5 μ s. Two machine cycles take 3.0 μ s.)

(b) 5.68 ms

The calculation uses the formula for the charging of a capacitor with an applied voltage and a series resistor:

$$V_{RST} = V_{CC}(1 - e^{-1(t/RC)})$$
$$2.5 = 5.0(1 - e^{-1(t/(10\mu F * 8.4K))})$$

and solving for t yields

$$t = 5.68 \text{ ms}$$

25. 4

26. \overline{PSEN} selects external EPROM. \overline{RD} and \overline{WR} select external RAMs.

27. 2FH

Figure 2-4 shows the addressable bit locations and the corresponding byte addresses.

28. 7BH

29.

Signal	Bit Address	Pin Number	Signal	Bit Address	Pin Number
P0.0	80H	39	P2.0	A0H	21
P0.1	81H	38	P2.1	A1H	22
P0.2	82H	37	P2.2	A2H	23
P0.3	83H	36	P2.3	A3H	24
P0.4	84H	35	P2.4	A4H	25
P0.5	85H	34	P2.5	A5H	26
P0.6	86H	33	P2.6	A6H	27
P0.7	87H	32	P2.7	A7H	28
P1.0	90H	1	P3.0	B0H	10
P1.1	91H	2	P3.1	B1H	11
P1.2	92H	3	P3.2	B2H	12
P1.3	93H	4	P3.3	B3H	13
P1.4	94H	5	P3.4	B4H	14
P1.5	95H	6	P3.5	B5H	15
P1.6	96H	7	P3.6	B6H	16
P1.7	97H	8	P3.7	B7H	17

30. (a) bit 7 in byte address 26H
(b) bit 7 in byte address 2EH
(c) bit 7 in byte address F0H

31. (a) bit 0 in byte address A8H
(b) bit 4 in byte address 80H
(c) bit 3 in byte address 2CH

32. SETB ACC.0

SETB exists in two forms:

```
SETB C
```

a one-byte instruction which sets the carry flag (implicitly specified in the opcode), and

```
SETB bit
```

a two-byte instruction which sets any bit-addressable location. The latter form requires the direct address of the bit. The solution is shown using the "dot operator", which allows a bit to be specified using the byte address of a bit-addressable location, followed by a period (or dot), followed by the bit position within the byte. The assembler converts this to the corresponding bit address.

Note that all bit-addressable special function registers have byte addresses with the least-significant three bits clear, or

aaaaa000

Substituting the bit position (specified in binary) into these three bits gives the correct bit address.

The answer shown above is equivalent to "SETB 0E0H" which explicitly provides the address of the least-significant bit in the Accumulator.

33. (a) P = 0
(b) P = 1
(c) P = 0

34. (a) P = 0
(b) P = 0
(c) P = 1

- 35.
- ```
MOV DPTR, #0100H
MOV A, R7
MOVX @DPTR, A
```

The only instruction that writes to external data memory is MOVX @DPTR,A. Values written to external data memory, therefore, must be transferred to the accumulator first.

- 36.
- ```
MOV    DPTR, #08F5H
MOVX   A, @DPTR
MOV    0F0H, A
```

37. 08H (PC low-byte) and 09H (PC high-byte)

The 8051's Stack Pointer is set to 07H upon reset. Also, the SP is pre-incremented for push operations and post-decremented for pop operations. The first write to the stack following a system reset (assuming the SP is left as is) is to location 08H, and the second is to location 09H.

CALL instructions push the PC on the stack prior to branching to the subroutine. By convention on the 8051, the PC high-byte is pushed first, and the PC low-byte is pushed second.

38. (a) C0H

The stack can grow as high as FFH, so the maximum size of the stack is 64 bytes.

- (b) On the 8031, this instruction is most likely a programming error, because the stack cannot exist above address 7FH – the highest memory location accessible using indirect addressing. (Note: The stack is accessed using indirect addressing using the instructions CALL, RET, RETI, PUSH, and POP. The stack pointer (SP) is the register used to access the stack.)
39. The initial value of the stack pointer after a system reset is 07H, so the stack will begin at address 08H and move “up” in memory. The register banks occupy locations 00H through 1FH, with register bank 0 at 00H-07H, register bank 1 at 08H-0FH, etc. The stack, therefore, overlaps the space assigned for register banks 1, 2, and 3. If a program uses these register banks, then the stack pointer must be initialized to a new value at the beginning of the program.

Any value 1FH or greater will do, as long as sufficient space is dedicated to the stack and as long as the stack does not exceed the highest indirectly accessible location (7FH on the 80x1, FFH on the 80x2). A minor, and unlikely, exception would be for a program that does not use the stack. In this case the stack pointer need not be initialized.

40. Power down mode can only be exited by a system reset; whereas, idle mode can be exited by system reset or any enabled interrupt.

41.

```

MOV     A,PCON      ;read PCON into A
ORL     A,#02H      ;set Power Down bit
MOV     PCON,A      ;write PCON with PD = 1
                        ;Power Down mode entered

```

The power control register is not bit-addressable, so setting bit 1 — the PD bit (see Table 2-4) — must use a byte transfer operation, as shown above.

If the previous content of PCON is of no concern, then this operation can be performed in a single instruction:

MOV PCON, #02H

42. See Figure 1.

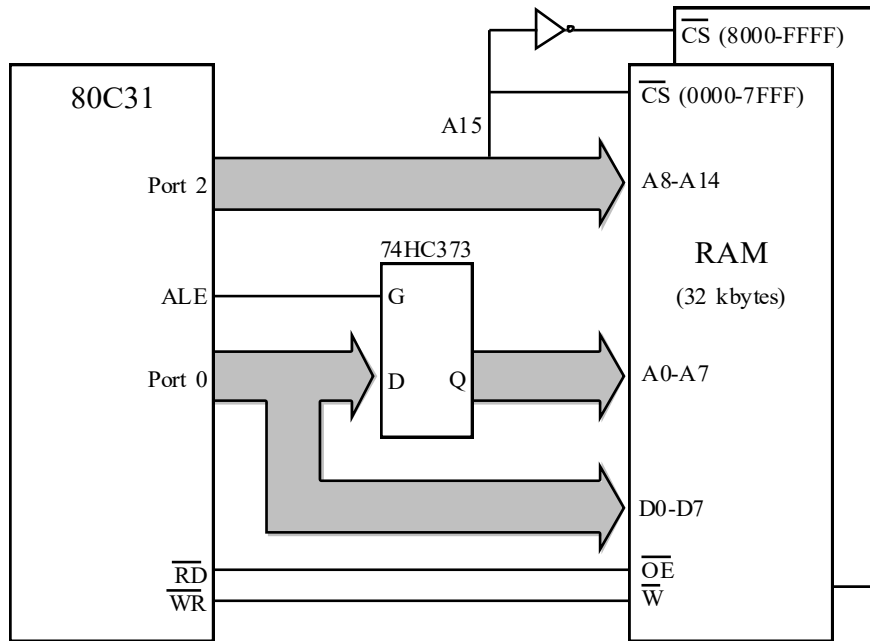


Figure 1. Interfacing RAMs to an 80C31

The interface uses $A_{15} = 0$ to select one RAM for addresses 0000H-7FFFH and $A_{15} = 1$ to select the other for addresses 8000H-FFFFH. The RAMs are selected only for accesses to external data memory since \overline{OE} and \overline{WE} connect to the 8051's \overline{RD} and \overline{WR} lines respectively. Recall that (external) code memory is selected via \overline{PSEN} .

43. A = 00H
B = 00H
Internal RAM location 30H = 33H
SP = 07H
44. The phrase “I/O expansion” refers to increasing the number of input/output lines of a microprocessor or a microcontroller.
45. Microcontrollers that use memory-mapped I/O would treat I/O devices like memory locations, and so all instructions that access memory would apply to these I/O devices as well. In contrast, some microcontrollers connect to I/O devices through I/O ports meant specially for them. In this case, special-purpose I/O instructions are required to access these I/O devices.
46. The External Access (\overline{EA}) signal on pin 31 should be tied low to signify that the 8051 executes programs from external ROM. Meanwhile, the Program Store Enable (PSEN)

pulses low during the fetch stage of an instruction. The program counter (PC) register contains the address of the next instruction to be executed, and upon reset, has the value of 00H which identifies the location of the first instruction to be fetched.

47. Even though the 8051 has 256 bytes of internal RAM, only the lower half is available for temporary storage of general data, whereas the upper half is reserved for special function registers. That's why we consider the effective size of internal data memory to be 128 bytes.
48. The stack is a sequence of locations in internal data memory that are used to temporarily store values in a last-in-first-out (LIFO) fashion. Meanwhile, the stack pointer is a register that contains the current location of the top of the stack.

